Changes approved 1/24/05 JWL

Amendments to the Specification

Please replace the paragraph beginning at page 8, line 18, with the following rewritten paragraph:

--The JG memory consists of up to eight bytes of memory. Each register consists of the components illustrated in FIG. 8. Control signals 442 and 444 activate the register and determine whether the JTAG controller is writing to or reading from the register. Memory bits 450-457 hold single bits, memory bit 450 being the least significant bit (LSB). Bit select multiplexer 460, bit address selector 462, BitByt multiplexer 464, ~~are~~ and BitByt selector 466 are used to select a particular bit for output, or to send an entire byte for output, depending on whether bits or bytes are to be shifted out. TDO/Bit 0 output 468 along with the outputs for the other bits are then sent to an ordinary memory multiplexer for output.--

Please replace the paragraph beginning at page 9, line 8, with the following rewritten paragraph:

--Bits are shifted in from the CUT and out to the CUT via TDO line 380 in SHIFT_DATAINOUT_STAT 434. Up to 8 bytes (256 bits) may be shifted in and out depending on the implementation of the CUT core. Bits shifted out to the CUT are addressed by the bit counter 350 via address multiplexer 300. For each bit shifted out to the CUT, one bit is shifted in ~~(310)~~ (320) from the CUT to the shift register ~~320~~ 310, as illustrated in FIG. 5.--